PoppyUp — Phase 1 Hardware Design

Wiring & Interconnect Diagram Set — Rev A (ADR v0.3), 2026-09-27

Status: DRAFT — FOR REVIEW. Logical wiring and connection diagrams — not to scale; no physical routing or cable lengths are implied unless a length is stated with its basis.

DRAWING INDEX

Sheet	Title	Rev	Scale
PU-W-000	Cover, index, legend, general notes, open items	A	NTS
PU-W-101	System interconnect — boards, modules, harnesses and external ports	A	NTS
PU-W-102	Power distribution wiring	A	NTS
PU-W-103	Embedded-controller control and sensor wiring	A	NTS
PU-W-104	CFexpress B mode-switch path — lane mux, clock mux, interlock, USB4 bridge	A	NTS
PU-W-201	Mezzanine J3 / J6 — 80-pin connection diagram	A	NTS
PU-W-202	Battery pack sub-assembly wiring	A	NTS
PU-W-203	External ports and M.2 module connector wiring	A	NTS
PU-W-204	Peripheral connector pinouts — OLED, button flex, pack, debug, fan, thermal switch	A	NTS
PU-W-301	Connection schedule	A	NTS

CONVENTIONS

General notes

1. Sheet size A3 landscape (420 × 297 mm), zones 1–8 across / A–F down. Lineweights: 0.50 mm borders and block outlines, 0.35 mm primary connections, 0.25 mm secondary, 0.18 mm leaders and dimensions.
2. Connection classes are shown by colour AND line type (legend, right) so monochrome prints remain readable. Junction dots mark intentional joins; crossings without a dot are not connected.
3. Equipment IDs: MB main board, RB reader daughterboard, PB pack PCB, SOM compute module, WIFI / NVME M.2 modules, OLED, BTNFLX button flex, ANTW0/1 Wi-Fi antennas, THSW thermal switch, CHASSIS. Connector refs (J1…) are those of docs/09 §9.
4. Connection IDs: W-nn off-board (cables, flexes, mated modules, bonds — schedule on PU-W-301 and PU_Connection-Schedule_Rev-A.csv); P-nn on-board power links (PU-W-102). Signal names follow docs/02 §8 and docs/09 §8.
5. Evidence classes in the schedule: Verified (stated in docs/00–13 or a public standard), Derived, Assumed (drafting proposal — confirm at schematic capture), TBD. Nothing here is a manufacturer pinout unless the standard is named.
6. Base / Pro SKU: items populated on the Pro SKU only (ASM2464PD, Port C PD controller TPS25750-C, TPS2121-class VBUS mux, NVMe) are marked 'Pro'; the PCB is common.
7. Layers in the SVG source: L-BORDER, L-TITLE, L-REFERENCE, L-EQUIPMENT, L-CONN-POWER/HS/CTRL/BUS/RF/BOND/REF/MECH, L-ANNOTATION, L-REVISION.

LEGEND

- POWER: Power (VBUS, VBAT, VSYS, rails)
- HS: High-speed data (PCIe, USB, USB4, MDI)
- CTRL: Control / discrete (GPIO, enables, detects)
- BUS: Serial bus (I²C, SMBus, SPI, UART)
- RF: RF coax (MHF4)
- BOND: Chassis / ground bond
- REF: Reserved, alternative or depopulated
- MECH: Direct mate (module in socket, no cable)
- Chassis ground (magnesium chassis, masked conversion-coated land)
- Signal / board ground
- Junction (intentional connection)
- PU-W-102 / P-05 — Off-sheet reference: sheet / connection ID
- BLOCK / PORT — Equipment block with port stub and port label
- Dashed outline: Pro-only population, reserved or TBD item

OPEN ITEMS AND SOURCE-DOCUMENT CONFLICTS FOUND WHILE DRAFTING (details: PU_Validation_Rev-A.md)

ID	Item	Conflict / gap	Docs
OI-1	Thermal switch rating	48 °C in 02 §8 / 06 §7.2 / 09 §7 vs '60 °C class, re-rated from 48 °C' in ADR 00 §3.5; location and interrupted circuit unspecified.	00, 02, 06, 09
OI-2	Slot eFuse current limits	09 §5.2: CFe B 2.5 / CFe A 1.5 / CFast 1.0 / SD 0.8 / µSD 0.5 A. 05 §3.2, §4: 2.0 / 1.2 / 1.2 / 0.5 / 0.3 A.	05, 09
OI-3	Pack connector family and current per pin	6-pin JST GH/XA (09) vs Molex Micro-Fit / JST GH (05); one pin each for PACK+/– must carry 5 A charge / 7 A system peaks; pack path stated 10 A cont. + 20 A fuse (09 §2.3) vs 10 A fuse (05).	05, 09
OI-4	Hall sensor location	On RB with mezzanine pin 66 (09 §1, §8.1) and on the MB J11 'Button/Hall flex' (09 §9.1); the 3D viewer already flags its position.	09, viewer
OI-5	AON LDO source	05 §4 feeds the 3.3 V AON LDO from VBAT; 09 §5.1 from VSYS.	05, 09
OI-6	VSYS bulk capacitance	2× 470 µF + 4× 22 µF (05 §10.2) vs 2× 220 µF + 10× 10 µF (09 §5.1).	05, 09
OI-7	1.8 V source	1 A buck on MB (09 §5.1, mezz pin 54) vs TLV75518 LDO with the readers (05 §5).	05, 09
OI-8	NTC channel allocation	02 §8 NTC[5:0]: SoM boss, switch, CFe B cage, Ethernet PHY, battery, internal air; 06 §6: skin #1, skin #2 (bottom band), front frame, internal air, battery ×2 via SMBus; 09 §7: SoM edge, ASM2812, RTL8126, CFe B cage, pack, spare; 10 BOM: ×4.	02, 06, 09, 10
OI-9	Interlock latch enable sense	09 §5.4 latches MUX_SEL with LE = NOT CFEB_PWR_EN_SENSE 'from the eFuse power-good', but the CFe B eFuse is on the RB and the mezzanine allocation (09 §8.1) has no PG/sense return pin — only the wired-OR SLOT_FAULT#. Either sense the EC's CFEB_PWR_EN on the MB or add a pin.	09
OI-10	SoM connector count	2× B2B (09 §1.1, §9.1 J1/J2) vs 3× B2B (04 §, 08 §3.2). Moot if board-down is selected (D12).	04, 08, 09
OI-11	RB length	180 × 38 mm (09 §1 table) vs 172 mm (09 §1.2, 08 §3.1, drawings).	08, 09
OI-12	Port C PD ownership	TPS25750-C owns CC with the ASM2464PD PD block passive (00 §3.4) — verify with ASMedia (02 §10).	00, 02
OI-13	USB-C SuperSpeed orientation handling	No document states how plug-flip is handled on Ports A (RK3588 USBDP PHY) and B (ASM3142): PHY lane select vs external SS mux. Drawn as 'orientation: TBD'.	—
OI-14	Reset pinhole switch	08 §7 places a sealed reset tact on the bottom face; no connector or EC signal is listed in 09 §9.1 / 02 §8. Drawn as MB-mounted, to EC GPIO (assumed).	02, 08, 09
OI-15	LED bar location and supply	On RB (09 §9.2 J7) with LED_DATA over mezzanine 67; 05 §5 conditions its supply on ≤ 100 mA from the AON LDO, else a 5 V driver — neither appears on the mezzanine allocation (3.3 V AON is not a mezzanine rail).	05, 09
OI-16	Wi-Fi antenna cable length	09 §4.2 caps the MHF4 cable at ≤ 120 mm; 07 §4.3 routes WIFI0 at ≈ 140–150 mm along the top rail (W-05).	07, 09

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
Cover, index, legend, general notes, open items Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py	**Sheet PU-W-000** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	**Status: DRAFT — FOR REVIEW** Sheet 1 of 10	Reviewed: — Approved: —

SYSTEM INTERCONNECT — boards, modules, harnesses, chassis bonds and external ports (logical, NTS)

RB — Reader daughterboard (8L, 172 × 38 mm, reader band)

Top edge, left→right: J5 CFast 2.0 | J1 CFexpress B | J2 CFexpress A | J3 SD UHS-II | J4 microSD
GL9755 · GL9750 · ASM1064 · 5× eFuse (TPS2596 class) · card-detect ×5 · Hall sensor (baseline, OI-4) · RB EEPROM

J7 LED bar — W-07 LED_DATA — on-RB LEDs / FPC alt. (TBD) — **LEDBAR — 5-segment RGB bar** — front top edge, over the slot row

GND (rail + cage pins) — W-18 RB GND via mounting rail + cage pins

J6 mezzanine (ADF6, female)

W-01 Samtec ADM6 / ADF6 80-pin, direct mate, stack 5–8 mm (height TBD)
CFe B Gen3/Gen4 ×2 + REFCLK + sidebands · CFe A ×1 · 3× Gen3 ×1 · 3.3 V slots / logic · 1.8 V · EC signals

PU-W-201 pin allocation

J3 mezzanine (ADM6, male)

ANTW0 — Wi-Fi flex, X 12–52 — W-05 MHF4 coax ≈140–150 mm (est.) — ANT0
ANTW1 — Wi-Fi flex, X 130–170 — W-06 MHF4 ≈60 mm (est.) — ANT1

MB — Main board (10L hybrid, 165 × 80 mm)

ASM2812 switch · PI3DBS16412 + HCSL clock mux · ASM2464PD (Pro) · ASM3142 · RTL8126 + magnetics
TPS25750 ×3 · TPS2121-class VBUS mux (Pro) · BQ25792 · bucks · TPM SLB9672 · nRF5340 EC + BLE chip antenna

OLED — 2.42" 128 × 64, SSD1309 — W-03 OLED FPC 30-pin — SPI · VDD 3.3 · VCC 12 V — J10 OLED FPC 30-pin

BTNFLX — button flex (front frame) — W-04 flex 6-pin (proposed) — BTN · ring LED · 3.3 V AON — J11 button flex 6-pin

J8 M.2 Key-E 2230 — Wi-Fi — W-11 mated in J8 — **WIFI — M.2 Key-E 2230, MT7925** — Wi-Fi 7 2×2; pcie2x1l1; BT held in reset; 2× MHF4 (I-PEX 20449) on the module

J9 M.2 M-key 2280 — NVMe (Pro) — W-12 mated in J9 (Pro) — **NVME — M.2 M-key 2280 SSD (Pro)** — socket J9 present, empty on Base

PACK — battery pack 2S2P 21700, 72 Wh — certified sub-assembly, behind screw-down door

PB — pack PCB (2L) — BQ40Z50-R2 · BQ294xx · 10 A fuse · 2× NTC

J1 — W-02 6-way pack harness — PACK± · SMBus · NTC · PRES# — J12 battery pack 6-pin

PACK– — W-20 pack – bond, one point — GND — pack – one-point bond

W-10 mated on J1 / J2 (B2B)

SOM — RK3588(J) compute module
Firefly Core-3588J (v0.2 default) / Forlinx FET3588-C / board-down RK3588J — decided at PoC exit (D12)
pcie3x4, pcie3x2, 3× Gen2, USB3 OTG0/1, USB2 ×2, SPI TPM, UART / I²C / GPIO to EC, 5.0 V SYS in

J15 / J16 spare PCIe Gen2 ×1 test headers (unpop.)

PU-W-202 pack · PU-W-204 J12 pinout

THSW — mechanical thermal switch — chassis inner wall, location TBD (OI-1) — W-08 2 leads, termination TBD — THERM_ALERT (OI-1) — TP-THSW thermal-switch leads (TBD)

FAN — tunnel fan (reserved envelope) — not fitted; decision at EVT exit (D5) — W-09 3-pin, unpopulated — J17 fan header (reserved)

PU-W-102 power · PU-W-103 EC signals · PU-W-104 CFe B path

J13 SoC UART · J14 EC SWD (Tag-Connect) — debug, unpopulated at PVT

GND — 8 screw bosses — W-17 8 bosses — **CHASSIS — Mg AZ91D die-cast** — ground reference; masked bare conversion-coated lands; Zn-Ni / Al fasteners only (D4)

J4–J7 shells / RJ45 frame — W-19 brackets / frame

J4 Port A — W-13 USB-C cable — **EXT-A — Port A host** — iPhone · Mac · PC · charger PD ≤ 100 W · USB3 Gen1

J5 Port B — W-14 USB-C cable — **EXT-B — Port B device** — SSD · tethered phone · USB cellular adapter

J6 Port C (Pro) — W-15 USB-C (USB4) — **EXT-C — Port C host (Pro)** — USB4 host / PD source blanked on Base

J7 RJ45 5GBASE-T — W-16 Cat 6A patch — **EXT-LAN — network** — 5GBASE-T, hinged door IP54 closed

PU-W-203 port and module wiring
PU-W-204 peripheral pinouts

Notes

1. Baseline ADR v0.3 (2026-09-27). Logical interconnect only: block positions and line lengths carry no physical meaning; no cable length is measured.
2. Dashed outlines = Pro-only population, reserved or TBD. Pro adds the NVMe in J9, Port C data (ASM2464PD) and Port C PD sink (TPS25750-C + TPS2121-class VBUS mux) on the same PCB; J6 receptacle is fitted on both SKUs and blanked on Base.
3. Harness lengths (W-02, W-05, W-06) are estimates from the docs/08 layout. RB-to-MB mezzanine stack height and ADM6/ADF6 variant are set when docs/08 fixes the spacing (09 §13).
4. Conflicts carried to PU-W-000: OI-3 pack connector family / current per pin; OI-4 Hall sensor on RB (mezzanine pin 66) vs on the J11 flex; OI-10 SoM connector count (2 vs 3 B2B). Not applicable if board-down is chosen (D12).
5. W-08 thermal switch: rating (48 °C vs 60 °C class, OI-1), location and interrupted circuit are fixed at EVT schematic release. J17 fan header stays unpopulated until the EVT-exit fan gate (D5).
6. Chassis bonds W-17…W-20: 8 MB screw bosses on exposed L1 GND rings, RB rail + cage pins, connector brackets / RJ45 frame, pack – at one point near the charger (09 §6). Bare conversion-coated Mg lands; never stainless into Mg (D4).
7. Detail sheets: PU-W-102 power, PU-W-103 EC signals, PU-W-104 CFe B mode-switch path, PU-W-201 mezzanine, PU-W-202 pack, PU-W-203 ports and modules, PU-W-204 pinouts, PU-W-301 schedule.

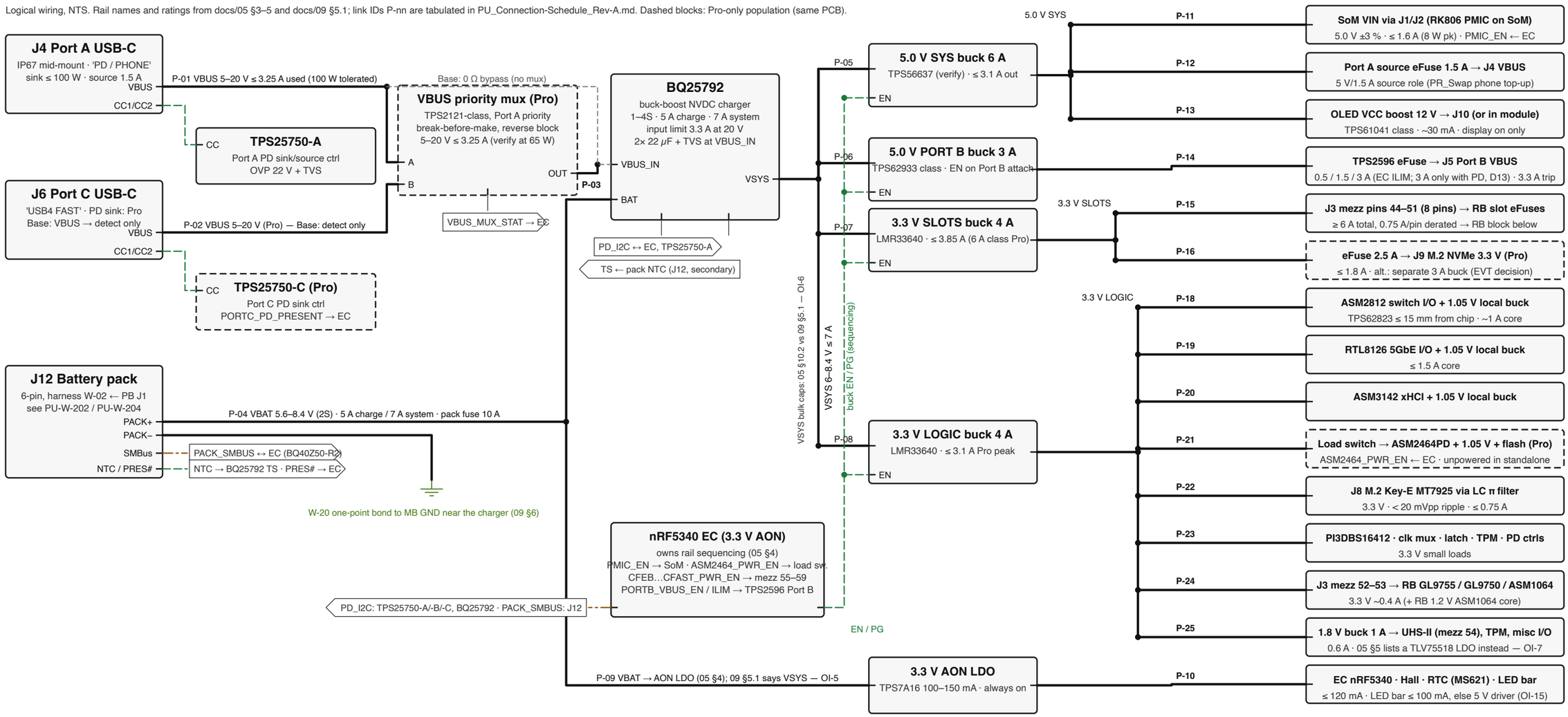
LEGEND — connection classes (colour + line type)

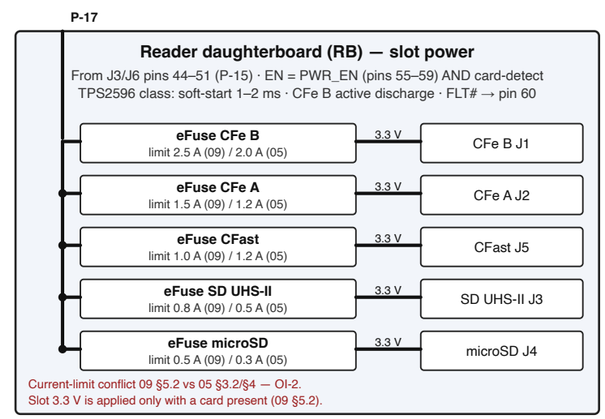
- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
System interconnect — boards, modules, harnesses and external ports	**Sheet PU-W-101** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Baseline: ADR v0.3 Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	**Status: DRAFT — FOR REVIEW** Sheet 2 of 10	Reviewed: — Approved: —

POWER DISTRIBUTION WIRING — inputs, charger, pack, rails, consumers (main board unless noted)

Logical wiring, NTS. Rail names and ratings from docs/05 §3–5 and docs/09 §5.1; link IDs P-nn are tabulated in PU_Connection-Schedule_Rev-A.md. Dashed blocks: Pro-only population (same PCB).





RAIL SUMMARY (09 §5.1, 05 §3.2)

Rail	Source	Rating	Consumers
VBUS_IN 5–20 V	Pro: TPS2121-class mux (A priority) · Base: Port A via 0 Ω	≤ 3.25 A	BQ25792 input
VSYS 6–8.4 V	BQ25792 NVDC output	≤ 7–8 A	all bucks, EC LDO (per 09)
5.0 V SYS	TPS56637 buck	6 A (≤ 3.1 A used)	SoM, Port A 1.5 A source, OLED boost
5.0 V PORT B	TPS62933 buck, ex-modem area	3 A	Port B VBUS via TPS2596 (EC ILIM)
3.3 V SLOTS	LMR33640 buck	4 A (6 A class Pro)	5 slot eFuses via mezz 44–51; NVMe eFuse (Pro)
3.3 V LOGIC	LMR33640 buck	4 A (≤ 3.1 A Pro)	ASM2812, RTL8126, Key-E, ASM3142, GL975x/ASM1064, PD ctrls, mux, TPM, ASM2464PD (Pro)
1.8 V	buck 1 A	0.6 A	UHS-II, TPM, misc I/O
1.05 / 1.2 V	point-of-load bucks TPS62823, one per chip	≤ 1.5 A each	ASM2812, RTL8126, ASM2464PD, ASM3142 cores
3.3 V AON	TPS7A16 LDO from VBAT (05) / VSYS (09)	100–150 mA	nRF5340, Hall, RTC, SMBus pull-ups

Notes

1. Sequencing (EC-controlled, 05 §4): 3.3 V AON always on → LOGIC → SLOTS (eFuses off) → 5.0 V SYS (SoM boots) → 5.0 V PORT B only on Port B attach (Rp set before VBUS) → slot eFuses as cards are detected. Power-down reverses; slot eFuses drop after unmount or the EC hard-cut timer.
2. PD attach (Pro, either port): Port A always wins at the mux; hand-over is break-before-make and the BQ25792 supplement mode rides the gap from the battery (no reset, VSYS droop ≤ 3–5 %). Input-current limit is re-programmed before the new input is made (05 §8).
3. Every rail's return is board GND; the battery negative is bonded to board GND at one point near the charger (W-20). Chassis bonds are on PU-W-101.
4. OI-2 slot eFuse limits differ between 09 §5.2 and 05 §3.2/§4 (both shown). OI-5 AON LDO source: VBAT (05 §4) vs VSYS (09 §5.1). OI-6 VSYS bulk capacitance differs (05 §10.2 vs 09 §5.1). OI-7 1.8 V: buck (09) vs LDO (05). OI-15 LED-bar supply: not on the mezzanine allocation.
5. Base SKU: TPS25750-C, the VBUS mux, the ASM2464PD load-switch path and the NVMe eFuse load are absent; Port A VBUS feeds the charger through a 0 Ω bypass (09 §1.1). All ratings marked (verify) in the source documents remain to be confirmed against datasheets before EVT schematic release.

LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set

Power distribution wiring
Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py

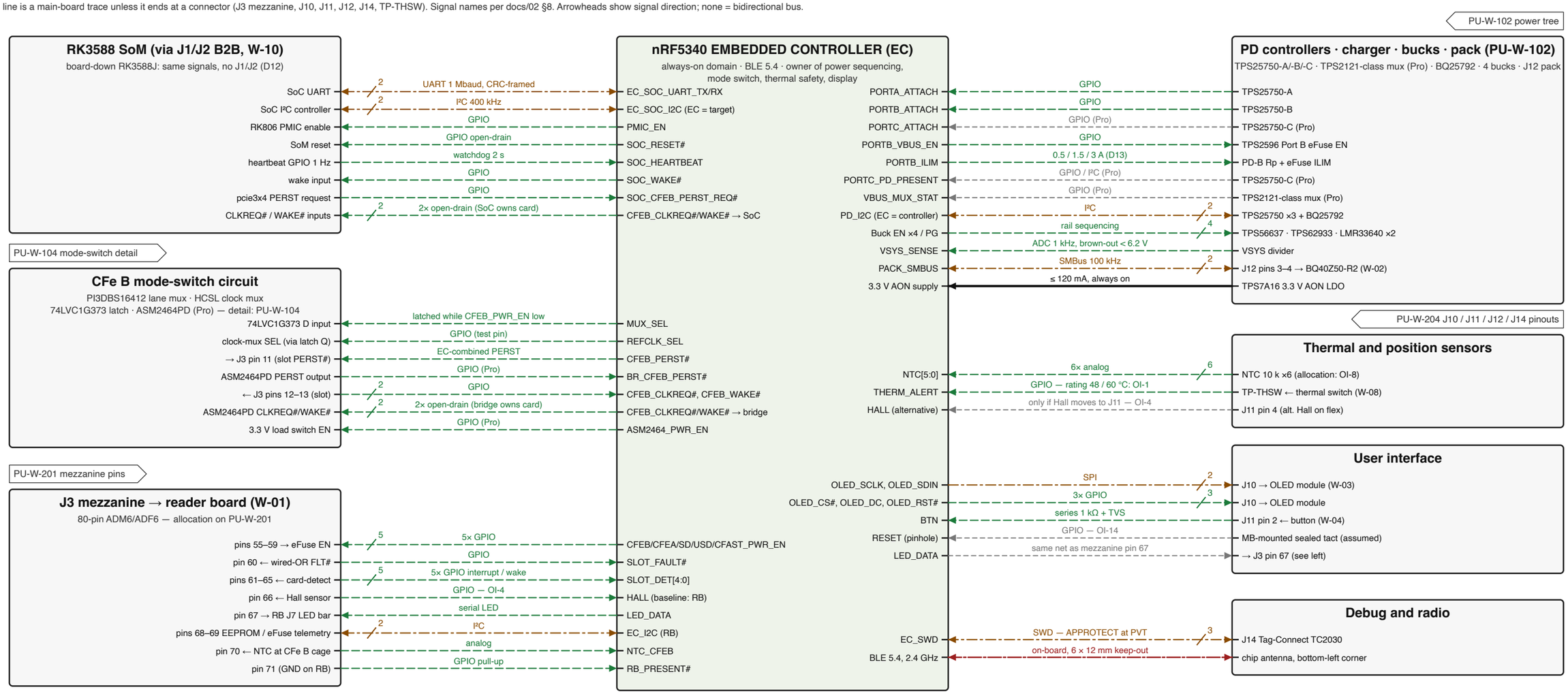
Scale: NTS — NOT TO SCALE
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9

Sheet PU-W-102
Rev A 2026-09-27
Status: DRAFT — FOR REVIEW
Sheet 3 of 10

Prepared: hw architecture (auto-generated set)
Reviewed: —
Approved: —

EMBEDDED-CONTROLLER (nRF5340) CONTROL AND SENSOR WIRING — signal owner view, NTS

Every line is a main-board trace unless it ends at a connector (J3 mezzanine, J10, J11, J12, J14, TP-THSW). Signal names per docs/02 §8. Arrowheads show signal direction; none = bidirectional bus.



Notes

1. The EC is the sole arbiter of mode-switch sequencing: MUX_SEL and REFCLK_SEL change only while CFEB_PWR_EN is low and CFEB_PERST# is asserted; the 74LVC1G373 latch makes this a hardware interlock independent of firmware (docs/02 §6.1, §8; docs/09 §5.4). Sideband signals PERST#/CLKREQ#/WAKE# terminate at the EC, which forwards them to the SoC or the ASM2464PD by mode.
2. SOC_HEARTBEAT is a 1 Hz toggle watched with a 2 s timeout; on loss the EC completes any hand-off autonomously, then asserts SOC_RESET# (docs/02 §6.7).
3. Thermal safety rule (D2, firmware): skin ≥ 52 °C, internal air ≥ 60 °C or battery ≥ 55 °C → THERMAL_PAUSE_REQ over UART, then PMIC_EN low; auto-resume at skin ≤ 42 °C and air ≤ 45 °C. THERM_ALERT from the mechanical switch is the firmware-independent backstop.
4. Port B supply policy (D13): PORTB_ILIM = min(user setting, 1.5 A) on battery; 3 A only while a PD contract is present on Port A (or Port C on Pro) — ADR 00 §3.5 requires ≥ 45 W for the 3 A step; drops to 1.5 A within 500 ms of losing external power.
5. Open items drawn as TBD/alternative: OI-1 thermal-switch rating and circuit; OI-4 Hall sensor on RB (mezzanine 66) vs J11 flex; OI-8 NTC channel allocation differs between docs/02, 06, 09 and 10; OI-14 reset pinhole switch has no connector or EC signal in docs/09 §9.1 / 02 §8.
6. Pro-only signals (PORTC_ATTACH, PORTC_PD_PRESENT, VBUS_MUX_STAT, BR_CFEB_PERST#, ASM2464_PWR_EN) are routed on every PCB; their far-end parts are depopulated on Base.

SIGNAL GROUP SUMMARY (source: docs/02 §8 table, model.EC_SIGNALS)

Group	Signals	Count	Class	Detail
SoM (J1/J2)	UART, I²C, PMIC_EN, SOC_RESET#, SOC_HEARTBEAT, SOC_WAKE#, SOC_CFEB_PERST_REQ#, 2× forwarded CLKREQ#/WAKE#	11	BUS / CTRL	—
Mode switch	MUX_SEL, REFCLK_SEL, CFEB_PERST#, BR_CFEB_PERST#, CFEB_CLKREQ#, CFEB_WAKE#, 2× forwarded to bridge, ASM2464_PWR_EN	9	CTRL	PU-W-104
Mezzanine J3	5× PWR_EN, SLOT_FAULT#, SLOT_DET[4:0], HALL, LED_DATA, I²C ×2, NTC_CFEB, RB_PRESENT#	17 pins (55–71)	CTRL / BUS	PU-W-201
PD / power	3× PORTx_ATTACH, PORTB_VBUS_EN / ILIM, PORTC_PD_PRESENT, VBUS_MUX_STAT, PD_I2C ×2, buck EN/PG ×4, VSYS_SENSE, PACK_SMBUS ×2, AON in	≈ 17	CTRL / BUS / POWER	PU-W-102
Sensors	NTC[5:0], THERM_ALERT, (HALL alt.)	7–8	CTRL	PU-W-204
UI	OLED SPI ×2 + CS/DC/RST, BTN, RESET, LED_DATA	7	BUS / CTRL	PU-W-204
Debug / radio	SWD (SWDIO, SWCLK, nRESET, SWO), BLE chip antenna	4 + RF	BUS / RF	PU-W-204

LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set

Embedded-controller control and sensor wiring
Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py

Scale: NTS — NOT TO SCALE
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9

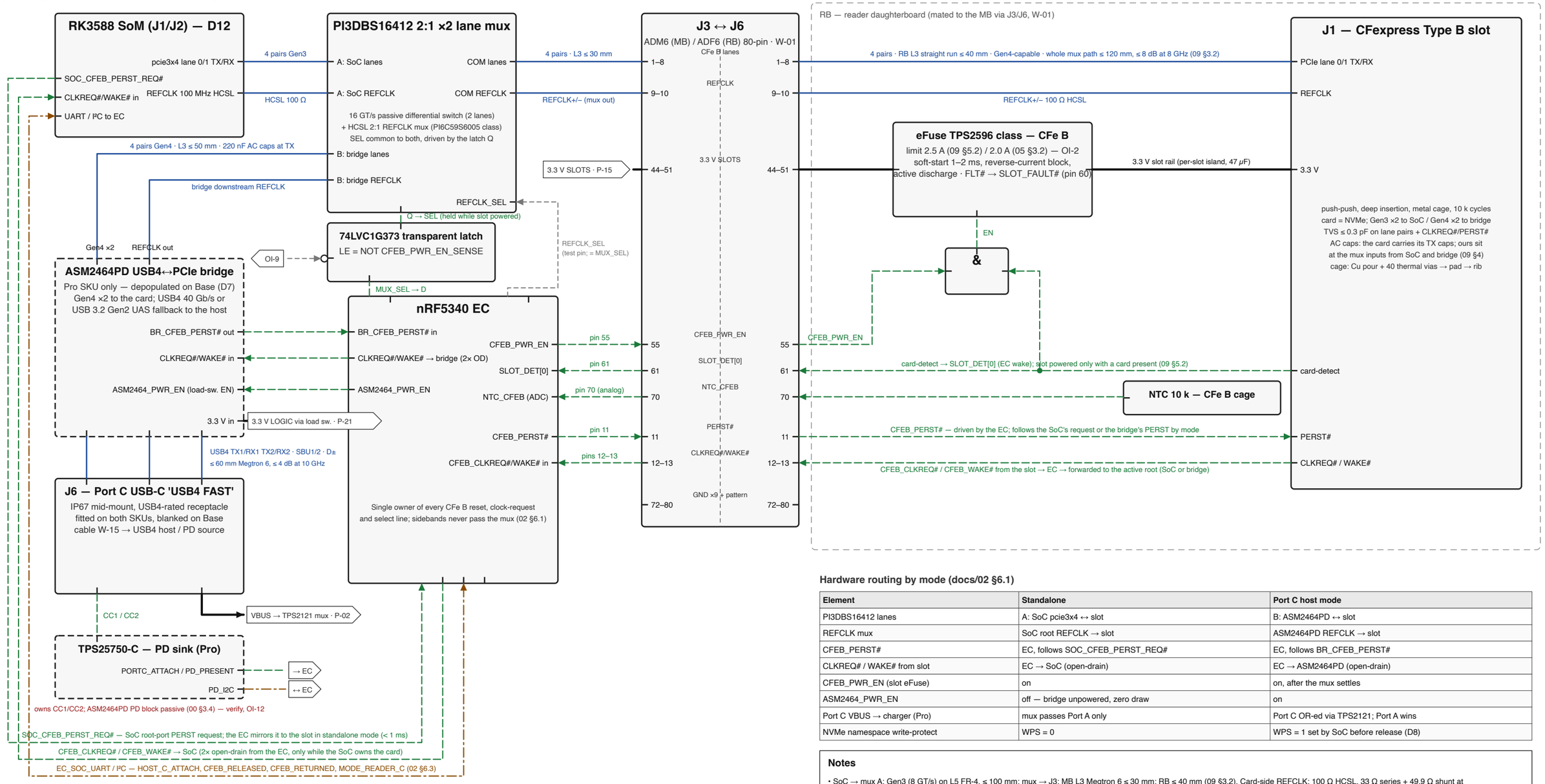
Sheet PU-W-103
Rev A 2026-09-27

Status: DRAFT — FOR REVIEW
Sheet 4 of 10

Prepared: hw architecture (auto-generated set)
Reviewed: —
Approved: —

CFEXPRESS B MODE-SWITCH PATH — lane mux, REFCLK mux, hardware interlock, USB4 bridge, Port C

Logical wiring, NTS. MB = main board, RB = reader daughterboard, EC = nRF5340. Pro-only population dashed (ASM2464PD, TPS25750-C, TPS2121-class mux). Sources: docs/02 §4.2, §6, §8; docs/09 §3.2, §4.1, §5.2, §5.4, §8.1.



Entering Port C host mode — EC-sequenced (docs/02 §6.3; target: card visible to the host in < 5 s)

1. Port C attach: TPS25750-C → PORTC_ATTACH → EC → UART HOST_C_ATTACH → SoC (≤ 50 ms). Pro: the Mac's VBUS is accepted at the charger through the priority mux from this moment.
2. SoC finishes the current part, checkpoints, fsyncs the job DB (≤ 1000 ms); unmounts the RO filesystem; Set Features 0x84 WPS = 1 if the card reports NWPC (≤ 50 ms) — else bridge WP (UAS) or user consent before flipping (02 §4.10).
3. SoC removes the PCI device, root port → D3, UART CFEB_RELEASED (≤ 400 ms; t ≤ 1500 ms cumulative).
4. EC: CFEB_PERST# low → CFEB_PWR_EN off, 200 ms dwell (active discharge, card < 0.3 V within 150 ms) → MUX_SEL = B, REFCLK_SEL = B (latch open while unpowered; 10 ms).
5. EC: ASM2464_PWR_EN on → bridge boots from SPI flash (300–500 ms) → CFEB_PWR_EN on, 100 ms → CFEB_PERST# released, now following BR_CFEB_PERST#.
6. Bridge trains Gen4 ×2 (≤ 300 ms); USB4 tunnel or USB 3.2 UAS enumeration; host mounts (1000–2000 ms); EC → SoC MODE_READER_C. Total ≈ 3.5–4.5 s. Exit reverses (02 §6.4): PERST# low, PWR_EN off 200 ms, bridge off, MUX_SEL = A, PWR_EN on, CFEB_RETURNED, SoC clears WPS, remounts RO.

Hardware routing by mode (docs/02 §6.1)

Element	Standalone	Port C host mode
PI3DBS16412 lanes	A: SoC pcie3x4 ↔ slot	B: ASM2464PD ↔ slot
REFCLK mux	SoC root REFCLK → slot	ASM2464PD REFCLK → slot
CFEB_PERST#	EC, follows SOC_CFEB_PERST_REQ#	EC, follows BR_CFEB_PERST#
CLKREQ# / WAKE# from slot	EC → SoC (open-drain)	EC → ASM2464PD (open-drain)
CFEB_PWR_EN (slot eFuse)	on	on, after the mux settles
ASM2464_PWR_EN	off — bridge unpowered, zero draw	on
Port C VBUS → charger (Pro)	mux passes Port A only	Port C OR-ed via TPS2121; Port A wins
NVMe namespace write-protect	WPS = 0	WPS = 1 set by SoC before release (D8)

Notes

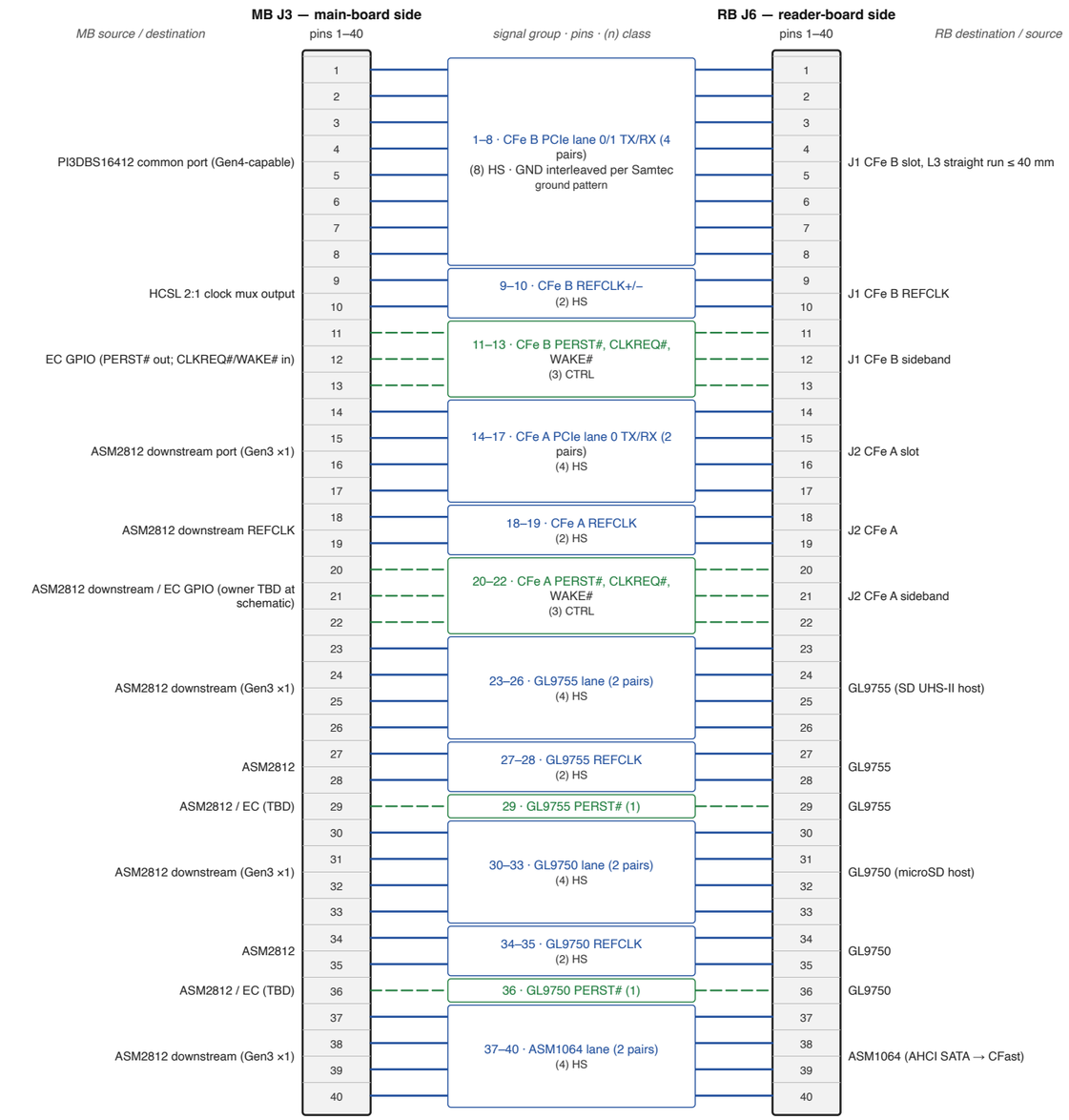
- SoC → mux A: Gen3 (8 GT/s) on L5 FR-4, ≤ 100 mm; mux → J3: MB L3 Megtron 6 ≤ 30 mm; RB ≤ 40 mm (09 §3.2). Card-side REFCLK: 100 Ω HCSL, 33 Ω series + 49.9 Ω shunt at the source, ≤ 0.5 ps RMS additive jitter through the mux (09 §4.1).
- Interlock (09 §5.4): D = EC MUX_SEL, LE = NOT CFEB_PWR_EN_SENSE, Q → both SEL pins — an unintended flip with a live card is impossible regardless of EC firmware. OI-9: 09 §5.4 takes the sense from the eFuse power-good, but that eFuse is on the RB and the 09 §8.1 mezzanine allocation has no PG return pin.
- ASM2464PD: 3.3 V LOGIC through a load switch (EN = ASM2464_PWR_EN), 1.05 V point-of-load buck ≤ 15 mm, SPI flash for its firmware; USB4 pairs to J6 use a ≤ 0.2 pF TVS (09 §5.1, §5.3). Base SKU: ASM2464PD, TPS25750-C and the TPS2121-class mux are depopulated; J6 is fitted and blanked and its VBUS pin goes only to attach detection (05 §7.5).

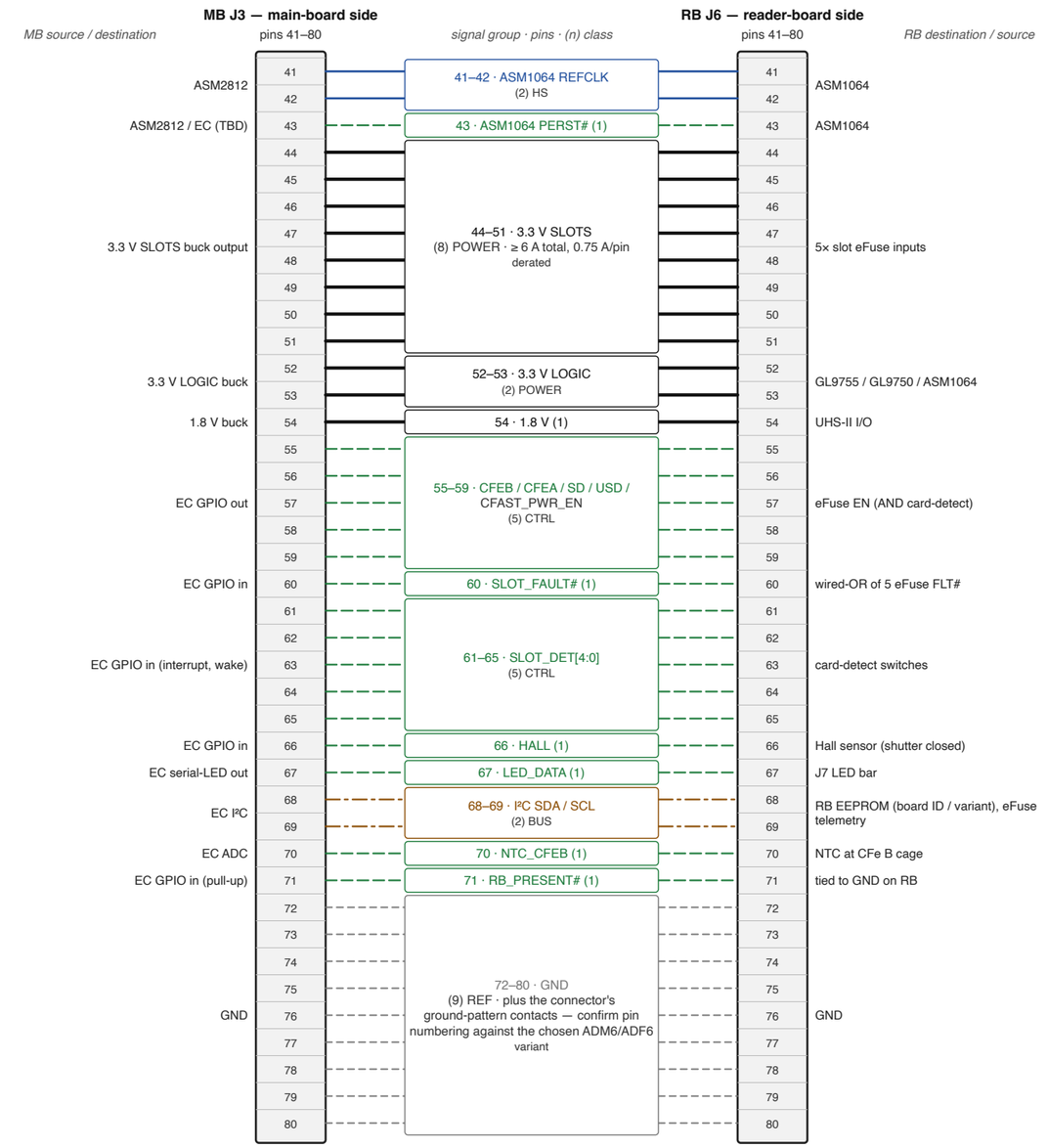
LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
CFexpress B mode-switch path — lane mux, clock mux, interlock, USB4 bridge	**Sheet PU-W-104** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Baseline: ADR v0.3	**Status: DRAFT — FOR REVIEW**	Reviewed: —
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	Sheet 5 of 10	Approved: —

MEZZANINE CONNECTION DIAGRAM — W-01: MB J3 (Samtec ADM6, male, 80 pos.) ↔ RB J6 (Samtec ADF6, female) — logical allocation per docs/09 §8.1, NTS





PIN SUMMARY BY CLASS

Class	Contents	Pins
HS	PCIe lanes and HCSL REFCLK pairs (CFe B Gen3/Gen4 ×2, CFe A ×1, GL9755, GL9750, ASM1064)	34
POWER	3.3 V SLOTS (8), 3.3 V LOGIC (2), 1.8 V (1)	11
CTRL	PERST# / CLKREQ# / WAKE#, PWR_EN ×5, SLOT_FAULT#, SLOT_DET[4:0], HALL, LED_DATA, NTC_CFEB, RB_PRESENT#	24
BUS	EC I²C to RB EEPROM and eFuse telemetry	2
REF	GND (9 listed pins + connector ground-pattern contacts)	9
Total		80

Notes

1. Logical allocation only (09 §8.1). Physical pin numbering, the one-GND-between-pairs pattern on the high-speed rows and the ADM6/ADF6 variant (stack height, ground-pattern option) are finalised from Samtec's S-parameter model at layout and when docs/08 fixes the RB-to-MB spacing (09 §13).
2. CFe B pairs (pins 1–8) form the Gen4 mux path: RB trace ≤ 40 mm on L3 with one reference plane each side and no layer change except the connector escape; mezzanine budget ≈ 0.5 dB at 8 GHz (09 §2.2, §3.2). Crosstalk target NEXT/FEXT ≤ –30 dB to 8 GHz (09 §12 item 6).
3. 3.3 V SLOTS on 8 pins (44–51) for ≥ 6 A total at a derated 0.75 A/pin (0.635 mm pitch). Slot eFuses and their card-detect gating sit on the RB; the eFuse limits differ between docs/05 and docs/09 (OI-2).
4. OI-9: the mode-switch interlock (74LVC1G373, 09 §5.4) wants CFEB_PWR_EN_SENSE from the CFe B eFuse power-good, but no PG / sense return pin exists in this allocation — only the wired-OR SLOT_FAULT# (60). Add a pin or sense the EC's CFEB_PWR_EN on the MB (see PU-W-104).
5. OI-4: HALL (66) assumes the Hall sensor is on the RB; docs/09 §9.1 also names a 'Button/Hall flex' on MB J11. One location must be chosen. LED_DATA (67) drives the RB LED bar (J7); the bar's supply rail is not a mezzanine rail (OI-15).
6. GND (72–80) is the listed count; the Samtec ground contacts in the shield / rows are additional and depend on the variant — confirm against the connector drawing at schematic capture.

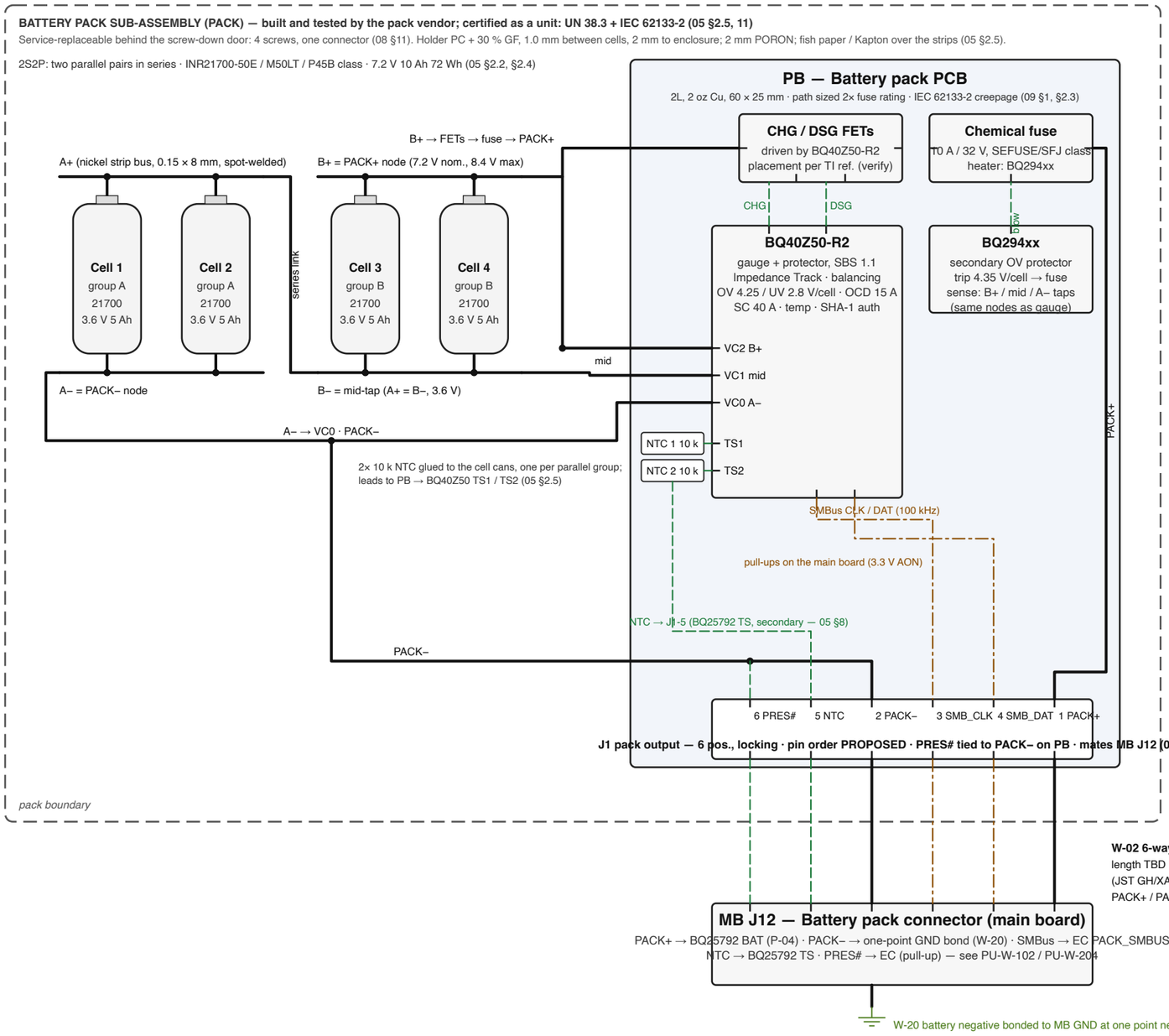
LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
Mezzanine J3 / J6 — 80-pin connection diagram Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py	**Sheet PU-W-201** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE	**Status: DRAFT — FOR REVIEW**	Reviewed: —
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	Sheet 6 of 10	Approved: —

BATTERY PACK SUB-ASSEMBLY WIRING — 2S2P 21700 pack, pack PCB (PB), harness W-02 to main board J12

Logical wiring, NTS. Sources: docs/05 §2.5, §8, §9, §12; docs/09 §1, §2.3, §9.3; docs/08 §11. FET placement, sense-resistor position and balance network per the TI BQ40Z50-R2 reference design — verify at schematic capture.



W-02 6-way discrete-wire pack harness, locking connector
length TBD (~60 mm est. from the docs/08 layout); connector family open — OI-3
(JST GH/XA class per 09 vs Molex Micro-Fit / JST GH per 05 vs Nano-Fit for 10 A per 09)
PACK+ / PACK– one pin each → ≥ 5 A/pin needed (5 A charge, 7 A system peak)

MB J12 — Battery pack connector (main board)
PACK+ → BQ25792 BAT (P-04) · PACK– → one-point GND bond (W-20) · SMBus → EC PACK_SMBUS
NTC → BQ25792 TS · PRES# → EC (pull-up) — see PU-W-102 / PU-W-204

W-20 battery negative bonded to MB GND at one point near the charger (09 §6)

J1 (PB) / J12 (MB) PIN ALLOCATION — signal list Verified (05 §2.5); pin order PROPOSED (Assumed)

Pin	Signal	Notes
1	PACK+	to BQ25792 BAT; ≥ 5 A/pin — one pin per rail is only viable on a ≥ 5 A/pin family (Micro-Fit 3.0 / Nano-Fit); JST GH (1 A) / XA (3 A) cannot carry 5 A on one pin
2	PACK–	one-point bond to MB GND near the charger
3	SMB_CLK	BQ40Z50-R2 SMBus, pull-ups on 3.3 V AON
4	SMB_DAT	
5	NTC	pack NTC to BQ25792 TS (secondary, 05 §8); primary NTCs read by BQ40Z50
6	PRES#	pack-present, tied to PACK– on PB (EC pull-up)

PROTECTION LAYERS AND PACK RULES (05 §8, §9, §12)

Layer	Rule / rating
Primary	BQ40Z50-R2 FETs: OV 4.25 V/cell, UV 2.8 V/cell, OCD 15 A, SC 40 A, temperature; cell balancing (bleed); Impedance Track SOH / cycle count; SHA-1 authentication
Secondary	BQ294xx opens the chemical fuse at 4.35 V/cell (independent of the gauge)
Charger	BQ25792 own OVP / OCP; charge 8.40 V (option 8.30 V longevity), 5.0 A fast charge (verify vs cell spec), pre-charge 500 mA < 6.0 V, termination 250 mA; JEITA 0–45 °C via BQ40Z50 NTCs (primary) and TS pin (secondary)
Cell temperature	2 NTCs; charge window 0–45 °C; discharge cut-off –20 / +60 °C by the protector; skin-temperature throttling acts first (06)
Fuse / path	10 A / 32 V chemical fuse (05 §2.5) — 09 §2.3 states '10 A continuous, 20 A fuse'; PCB traces sized for 2× fuse rating — reconcile (OI-3)
Mechanical	PC+GF holder, 2 mm PORON drop isolation, fish paper / Kapton; UN 38.3 T3/T4/T6 on the sub-assembly
Low battery	5 % graceful pause, 3 % EC hard cut, cell UVLO 2.8 V (pack 5.6 V); RTC kept by MS621 coin cell on the MB (05 §10.1)
Transport	≤ 100 Wh (72 Wh); ≤ 30 % SoC for air freight of finished goods, IATA PI 967 Section II label; Wh statement etched on the bottom face

Notes

1. The pack is permanently in circuit (NVDC): it is the hold-up for PD unplug and for the Pro Port A / Port C mux hand-over; no supercapacitor (05 §10.2).
2. Only PACK+, PACK–, SMBus, one NTC and PRES# leave the pack. The gauge reads the two cell-group NTCs; the MB reads one of them on the charger TS pin as a secondary check (05 §8).
3. OI-3: connector family and per-pin current, fuse rating (10 A vs 20 A) and pack-path continuous rating (10 A per 09 §2.3) are inconsistent between 05 and 09 — fix before the pack RFQ.
4. Cell make/model is a class choice (05 §2.4); the golden-image learning cycle and chemistry ID are set per cell type at PVT (05 §9).

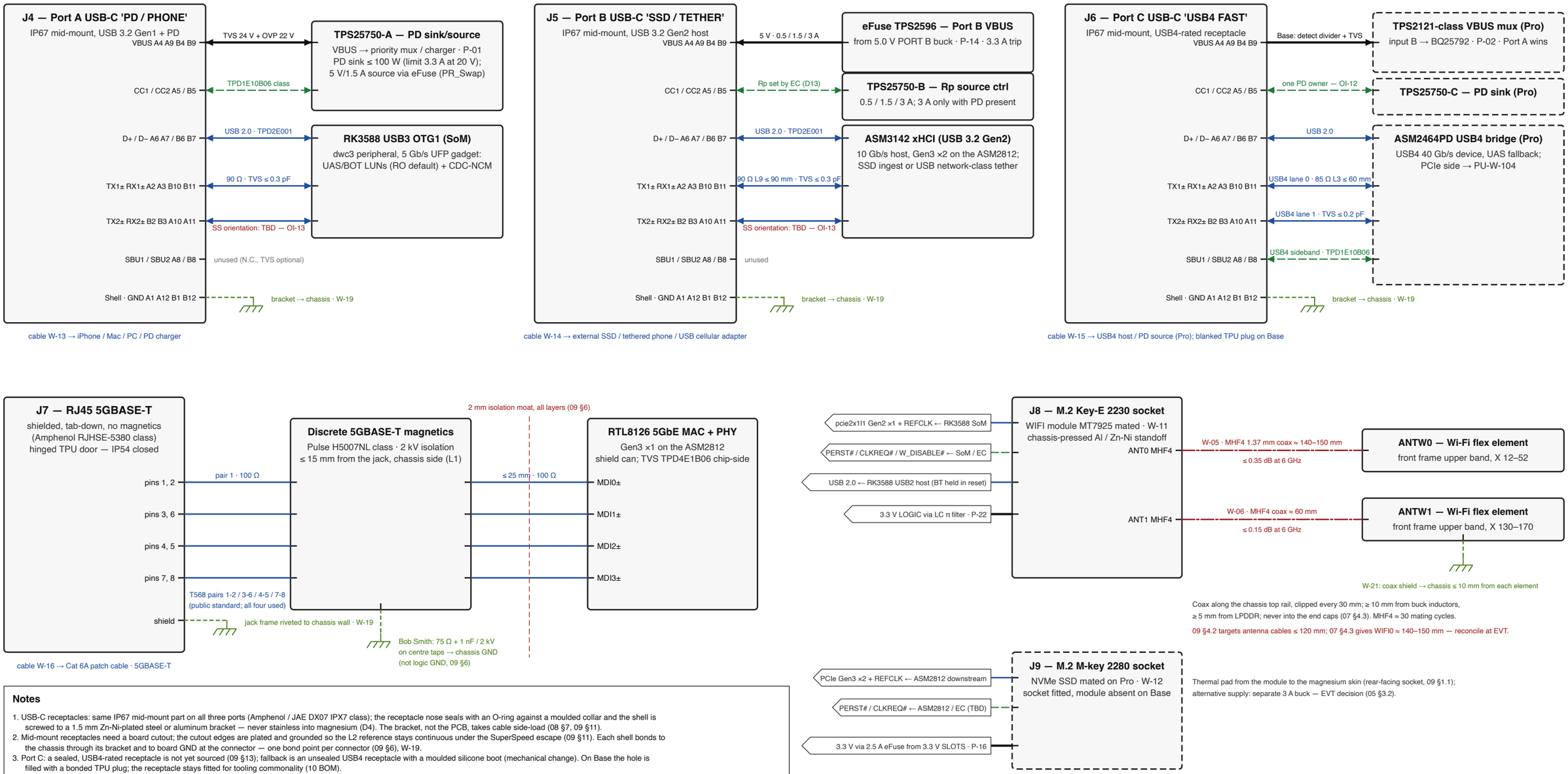
LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
Battery pack sub-assembly wiring Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py	**Sheet PU-W-202** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	**Status: DRAFT — FOR REVIEW** Sheet 7 of 10	Reviewed: — Approved: —

EXTERNAL PORTS AND M.2 MODULE CONNECTOR WIRING — Ports A / B / C (USB-C), RJ45, M.2 Key-E (Wi-Fi), M.2 M-key (NVMe)

Logical connector wiring, NTS. USB-C pin names per the USB Type-C specification (signal groups, both orientations wired); M.2 shown as signal groups only. Pro-only population dashed. Sources: docs/00 §3.3–3.4; docs/02 §4.5; docs/05 §7; docs/08 §7; docs/09 §3.4–3.5, §5.3, §6, §9.1, §11, §13.



Notes

1. USB-C receptacles: same IP67 mid-mount part on all three ports (Amphenol / JAE DX07 IPX7 class); the receptacle nose seals with an O-ring against a moulded collar and the shell is screwed to a 1.5 mm Zn-Ni-plated steel or aluminum bracket — never stainless into magnesium (D4). The bracket, not the PCB, takes cable side-load (08 §7, 09 §11).
2. Mid-mount receptacles need a board cutout; the cutout edges are plated and grounded so the L2 reference stays continuous under the SuperSpeed escape (09 §11). Each shell bonds to the chassis through its bracket and to board GND at the connector — one bond point per connector (09 §6), W-19.
3. Port C: a sealed, USB4-rated receptacle is not yet sourced (09 §13); fallback is an unsealed USB4 receptacle with a moulded silicone boot (mechanical change). On Base the hole is filled with a bonded TPU plug; the receptacle stays fitted for tooling commonality (10 BOM).
4. SuperSpeed plug-orientation handling (RK3588 USBDP PHY lane select vs external SS mux on Ports A/B) is not stated in any document — OI-13. Both TX/RX pair sets are wired to the receptacle as the Type-C spec requires.
5. ESD / TVS classes (09 §5.3): SS pairs ≤ 0.3 pF 4-ch (TPD4E05U06 / RClamp0524P class); USB4 port ≤ 0.2 pF (TPD4E02B04 class); CC and SBU TPD1E10B06 class, 22 V-tolerant on CC; VBUS TVS 24 V standoff + OVP 22 V; D± TPD2E001; RJ45 TPD4E1B06 on the chip side of the magnetics.
6. RJ45: T568 pair assignment is the public standard; 5GBASE-T (IEEE 802.3bz) uses all four pairs; PoE-in is not supported; intra-pair skew ≤ 50 ps (09 §12 item 8). Discrete magnetics because the jack needs a chassis-anchored shroud and gasket (09 §3.5).
7. M.2 sockets: 75-position, 4.2 mm; pin numbers per the PCI-SIG M.2 specification are not reproduced here. Wi-Fi module antenna connectors face the board edge nearest the front-frame antennas (09 §4.2); the 3.3 V LOGIC feed to the Key-E slot carries an LC π filter for < 20 mVpp ripple (05 §5).

LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
External ports and M.2 module connector wiring Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py	**Sheet PU-W-203** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	**Status: DRAFT — FOR REVIEW** Sheet 8 of 10	Reviewed: — Approved: —

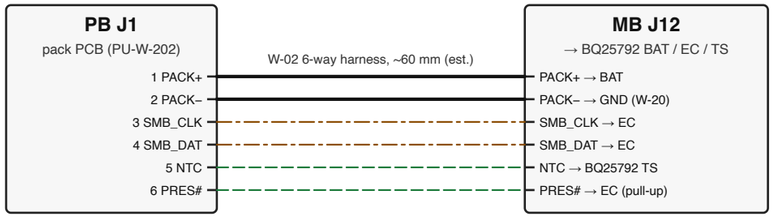
PERIPHERAL CONNECTOR PINOUTS — OLED (J10), button flex (J11), battery pack (J12 / PB J1), debug (J13, J14), fan (J17), thermal switch (TP-THSW) — NTS

Pin numbers marked Assumed are drafting proposals to be fixed at EVT schematic capture; none are manufacturer pinouts except where the standard is named. Signal lists come from docs/02 §8, 05 §2.5/§5, 09 §9.1.

J12 (MB) ↔ J1 (PB) — battery pack harness W-02

Status: Assumed (pin order); signal list Verified 05 §2.5

Pin	Signal	Note
1	PACK+	to BQ25792 BAT; ≥ 5 A/pin — one pin per rail is only viable on a ≥ 5 A/pin family (Micro-Fit 3.0 / Nano-Fit); JST GH (1 A) / XA (3 A) cannot carry 5 A on one pin
2	PACK–	one-point bond to MB GND near the charger
3	SMB_CLK	BQ40Z50-R2 SMBus, pull-ups on 3.3 V AON
4	SMB_DAT	
5	NTC	pack NTC to BQ25792 TS (secondary, 05 §8); primary NTCs read by BQ40Z50
6	PRES#	pack-present, tied to PACK– on PB (EC pull-up)



PACK+/– on one pin each → connector family must be ≥ 5 A/pin (OI-3)

J13 — SoC debug UART (SoC side, not EC)

Status: Assumed — proposal (unpopulated at PVT)

Pin	Signal	Note
1	GND	
2	SOC_UART_TX	1.8 V or 3.3 V level per SoM (verify)
3	SOC_UART_RX	
4	N.C. / VREF	

J14 — EC SWD, Tag-Connect TC2030 footprint (no component)

Status: Per Tag-Connect TC2030-CTX standard layout (verify against footprint drawing)

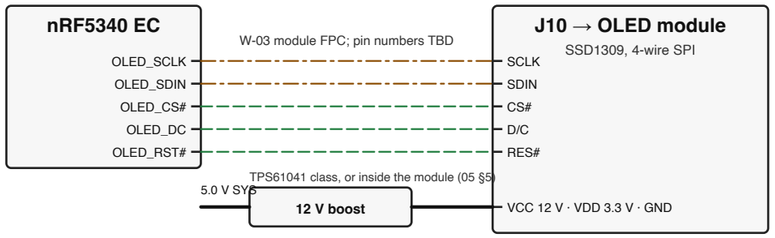
Pin	Signal	Note
1	VTref 3.3 V AON	
2	SWDIO	
3	nRESET	
4	SWCLK	
5	GND	
6	SWO	

J14 pin order per Tag-Connect TC2030-CTX ARM Cortex layout (public) — verify against the footprint drawing at layout.

J10 — OLED module FPC (W-03), 30-pin 0.5 mm

Status: Signals Verified (02 §8, 05 §5); pin numbers TBD per SSD1309 module datasheet

Pin	Signal	Note
—	GND	
—	VDD 3.3 V	logic
—	VCC 12 V	OLED panel supply (boost on MB or in module)
—	OLED_SCLK	SPI
—	OLED_SDIN	SPI MOSI
—	OLED_CS#	
—	OLED_DC	data/command
—	OLED_RST#	
—	(remaining pins)	per module: BS0–BS2 interface select tied for 4-wire SPI, VCOMH/IREF/VLSS caps, N.C.



J17 — fan header, reserved (W-09), unpopulated

Status: TBD — proposal

Pin	Signal	Note
1	GND	
2	FAN_V+	rail TBD (5.0 V SYS or VSYS)
3	FAN_PWM/TACH	EC GPIO (TBD)

TP-THSW — mechanical thermal switch leads (W-08)

Status: TBD

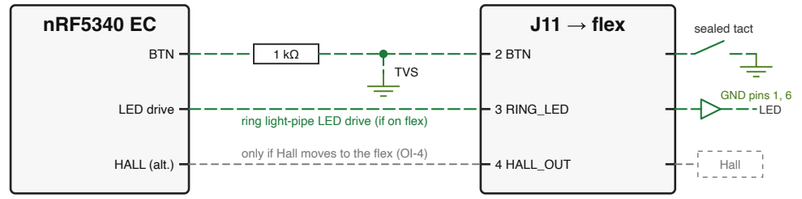
Pin	Signal	Note
1	THERM_ALERT	to EC GPIO (pull-up); switch contact
2	GND / interrupted circuit	circuit interrupted at trip is TBD (06 §12 item 10)

Rating 48 °C (docs/02, 06, 09) vs 60 °C class (ADR 00 §3.5) — OI-1; location and interrupted circuit fixed at EVT schematic release.

J11 — button flex (W-04), 6-pin 0.5 mm FPC

Status: Assumed — proposal

Pin	Signal	Note
1	GND	
2	BTN	sealed tact to GND; series 1 kΩ + TVS on MB
3	BTN_RING_LED	ring light-pipe LED (if on flex; else N.C.)
4	HALL_OUT	only if the Hall sensor moves to the flex — baseline: N.C. (Hall on RB, mezz pin 66)
5	3V3_AON	
6	GND	



3.3 V AON on pin 5 feeds the LED / Hall (if fitted); GND on pins 1 and 6; series 1 kΩ + TVS on the MB side (09 §5.3).

Cable and option notes

- W-05 / W-06 — Wi-Fi antenna coax: 2× MHF4 (I-PEX 20449) 1.37 mm, module (M.2 Key-E, X 140–162) → flex elements in the front frame upper band. WIFI0 ≈ 140–150 mm along the chassis top rail (≤ 0.35 dB at 6 GHz); WIFI1 ≈ 60 mm (≤ 0.15 dB). ~30 mating cycles; clipped every 30 mm; ≥ 10 mm from buck inductors; shield to chassis within 10 mm of the element (docs/07 §4.3). Lengths are estimates, not measured.
- W-07 — LED bar: baseline 5× addressable RGB LEDs on the reader board at RB J7, driven by LED_DATA over mezzanine pin 67; alternative is a 4-pin FPC to a light-guide flex (decide at industrial design). Supply: 3.3 V AON if peak ≤ 100 mA, else an LED driver from 5 V SYS (docs/05 §5) — neither rail is on the mezzanine allocation (OI-15).
- W-09 — fan header J17 is a reserved footprint only; the fan decision is taken at the EVT-exit gate (D5). Supply rail and control signal are TBD.
- W-08 — the thermal switch has no connector in docs/09 §9.1; TP-THSW is a placeholder for solder pads or a 2-pin header. The switch must interrupt a circuit where its trip temperature means a fault (charge path / pack region), not the SoM boss (docs/06 §12 item 10).
- OI-3 — pack harness: one pin each for PACK+ and PACK– must carry 5 A charge and 7 A system-path peaks; JST GH (1 A/pin) and XA (3 A/pin) cannot — Molex Micro-Fit 3.0 / Nano-Fit class or two pins per rail (then 8 positions). Pack path rating 10 A cont. / 20 A fuse (09 §2.3) vs 10 A fuse (05 §2.5) to reconcile.

LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set		
Peripheral connector pinouts — OLED, button flex, pack, debug, fan, thermal switch	**Sheet PU-W-204** Rev A 2026-09-27	Prepared: hw architecture (auto-generated set)
Scale: NTS — NOT TO SCALE Baseline: ADR v0.3	**Status: DRAFT — FOR REVIEW**	Reviewed: —
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9	Sheet 9 of 10	Approved: —

CONNECTION SCHEDULE — off-board connections (cables, flexes, mated modules, bonds)

Same data as PU_Connection-Schedule_Rev-A.csv / .md; on-board power links P-01…P-25 are tabulated in the .md and drawn on PU-W-102. Lengths are estimates from the docs/08 layout unless stated; none are measured.

ID	From	To	Medium	Signal / service	Class	Length	Status	Source	Sheets
W-01	MB J3	RB J6	Direct mate, Samtec ADM6/ADF6 80-pin, stack 5–8 mm	CFe B Gen3/Gen4 ×2 + REFCLK + sidebands; CFe A ×1; 3× Gen3 ×1 (GL9755/GL9750/ASM1064) + REFCLKs + PERST#; 3.3 V slots (8 pins) / 3.3 V logic (2) / 1.8 V (1); 5× PWR_EN; SLOT_FAULT#; SLOT_DET[4:0]; HALL; LED_DATA; I²C; NTC_CFEB; RB_PRESENT#; GND	HS	0 (mated)	Verified	09 §8.1	101 201
W-02	PB J1	MB J12	6-way discrete-wire pack harness with locking connector	PACK+, PACK–, SMBus CLK, SMBus DAT, NTC, PRES#	POWER	TBD (~60 mm est.)	Verified	05 §2.5, 09 §9.1	101 202 204
W-03	OLED FPC	MB J10	Module-supplied 30-pin 0.5 mm FPC	OLED_SPI (SCLK, SDIN), OLED_CS, OLED_DC, OLED_RST, VDD 3.3 V, VCC 12 V (boost, on MB or in module — 05 §5), GND	BUS	module tail	Verified	02 §8, 09 §9.1, 05 §5	101 204
W-04	BTNFLX FPC	MB J11	6-pin 0.5 mm FPC (front-frame flex)	BTN, button ring LED (if on flex), HALL (only if the Hall sensor is on the flex — conflict, see notes), 3.3 V AON, GND	CTRL	TBD	Assumed	09 §9.1 (J11 'Button/Hall flex'), 09 §1 (Hall on RB), 09 §8.1 pin 66	101 204
W-05	WIFI ANT0	ANTW0 PIG	MHF4 (I-PEX 20449) 1.37 mm coax	Wi-Fi chain 0, 2.4 / 5 / 6 GHz	RF	140–150 mm (est.)	Verified	07 §4.3	101 203
W-06	WIFI ANT1	ANTW1 PIG	MHF4 (I-PEX 20449) 1.37 mm coax	Wi-Fi chain 1, 2.4 / 5 / 6 GHz	RF	≈ 60 mm (est.)	Verified	07 §4.3	101 203
W-07	RB J7	LEDBAR —	On-board LEDs (baseline) or 4-pin FPC to light-guide flex (alternative)	LED_DATA (serial addressable), 3.3 V AON or 5 V (TBD, 05 §5 LDO note), GND	CTRL	—	TBD	09 §9.2 J7, 09 §1, 05 §5	101 204
W-08	THSW LEADS	MB TP-THSW	2 discrete leads, termination TBD	THERM_ALERT to EC; contact in series with a circuit TBD (charge path / pack region, 06 §12 item 10)	CTRL	TBD	TBD	00 §3.5, 02 §8, 06 §7.2/§12	101 103
W-09	MB J17	FAN —	Reserved 3-pin 1.25 mm header, unpopulated	Fan supply (rail TBD), GND, TACH/PWM (TBD)	REF	—	TBD	09 §9.1, ADR D5	101 204
W-10	SOM —	MB J1	Direct mate, SoM B2B connector set + 2× M2 retention screws	pcie3x4 (Gen3 ×2 used), pcie3x2 (Gen3 ×2), pcie2x1I0/I1/I2, USB3 OTG0/OTG1, USB2 host ×2, SPI (TPM), UART/I²C/GPIO to EC, 5.0 V SYS in, GND	MECH	—	Verified	02 §3, 09 §9.1, §11	101
W-11	WIFI —	MB J8	Direct mate, M.2 Key-E socket + chassis-pressed standoff	PCIe Gen2 ×1 (pcie2x1I1) + REFCLK + PERST#/CLKREQ#/W_DISABLE#, USB 2.0 (BT, held in reset), 3.3 V LOGIC via LC π filter, GND	MECH	—	Verified	02 §4.4, 05 §5, 09 §11	101 203
W-12	NVME —	MB J9	Direct mate, M.2 M-key socket + chassis-pressed standoff (Pro)	PCIe Gen3 ×2 from ASM2812 + REFCLK + PERST#/CLKREQ#, 3.3 V via 2.5 A eFuse from 3.3 V SLOTS (or separate 3 A buck — EVT decision), GND	MECH	—	Verified	02 §4.3, 05 §3.2/§4, 09 §11	101 203
W-13	MB J4	EXT-A —	User cable, USB-C	USB 3.2 Gen1 device (RK3588 OTG1) + USB 2.0; PD sink 5–20 V ≤ 100 W accepted (input limit 3.3 A at 20 V); PD source 5 V/1.5 A (PR_Swap option)	HS	—	Verified	00 §3.3/3.4, 05 §7	101 203
W-14	MB J5	EXT-B —	User cable, USB-C	USB 3.2 Gen2 host (ASM3142) + USB 2.0; 5 V source 0.5 / 1.5 / 3 A (Rp set by EC; 3 A only with external PD present, D13)	HS	—	Verified	00 §3.3/3.4, 05 §7.4	101 203
W-15	MB J6	EXT-C —	User cable, USB-C (USB4 40 Gb/s rated)	USB4 device (ASM2464PD, USB 3.2 Gen2 UAS fallback) — Pro only; PD sink 5–20 V ≤ 3.25 A via priority mux — Pro only; Base: receptacle blanked, VBUS to attach-detect only	HS	—	Verified	00 §3.4, 05 §7.5	101 203
W-16	MB J7	EXT-LAN —	Cat 6A patch cable	5GBASE-T, 4 MDI pairs through discrete magnetics; hinged door (IP54 closed)	HS	—	Verified	00 §5, 09 §3.5, 08 §7	101 203
W-17	MB GND	CHASSIS —	8× screw bosses on exposed L1 GND rings (6 vias each); masked bare conversion-coated Mg; Zn-Ni steel or Al screws	Chassis ground bond	BOND	—	Verified	09 §6, 08 §4.1	101
W-18	RB GND	CHASSIS —	RB mounting rail + 5 cage pins	Chassis ground bond; shutter and connector cages grounded to RB GND	BOND	—	Verified	09 §6, 08 §12 step 5	101
W-19	MB J4/J5/J6/J7 shells	CHASSIS —	Receptacle brackets (Zn-Ni steel / Al) and RJ45 frame riveted to chassis wall	Single-point-per-connector chassis bond; shells also to board GND at the connector	BOND	—	Verified	09 §6, 08 §7	101 203
W-20	PB PACK–	MB GND	One-point bond near the charger	Battery negative reference	BOND	—	Verified	09 §6	101 202
W-21	ANTW0 shield	CHASSIS —	Coax shield to chassis at the element end (feed PCB / EMI strip), within 10 mm of the element	RF ground	BOND	—	Verified	07 §4.3	203

Status: Verified = stated in the design package (docs/00–13); Assumed = drafting proposal to confirm at schematic capture; TBD = open. Class per legend. Sheet numbers are PU-W-xxx.

LEGEND — connection classes (colour + line type)

- Power (VBUS, VBAT, VSYS, rails)
- High-speed data (PCIe, USB, USB4, MDI)
- Control / discrete (GPIO, enables, detects)
- Serial bus (I²C, SMBus, SPI, UART)
- RF coax (MHF4)
- Chassis / ground bond
- Reserved, alternative or depopulated
- Direct mate (module in socket, no cable)

PoppyUp — Phase 1 Hardware Design — Wiring & Interconnect Diagram Set

Connection schedule
Baseline: ADR v0.3 Generated from wiring/model.py + wiring/build.py

Scale: NTS — NOT TO SCALE
Units: mm where dimensioned Signal names per docs/02 §8, docs/09 §8–9

Sheet PU-W-301
Rev A 2026-09-27
Status: DRAFT — FOR REVIEW
Sheet 10 of 10

Prepared: hw architecture (auto-generated set)
Reviewed: —
Approved: —